National Semiconductor

LH0005/LH0005A Operational Amplifier

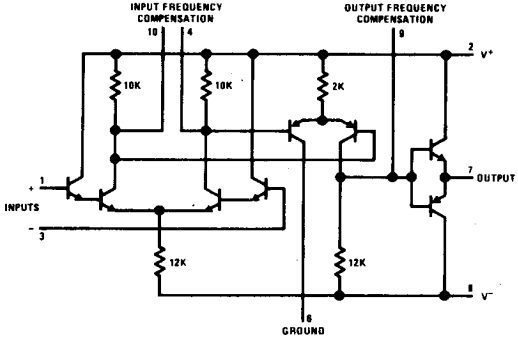
General Description

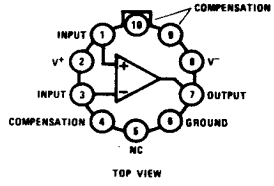
The LH0005/LH0005A is a hybrid integrated circuit operational amplifier employing thick film resistors and discrete silicon semiconductors in its design. The select matching of the input pairs of transistors results in low input bias currents and a very low input offset current, both of which exhibit excellent temperature tracking. In addition, the device features:

- Very high output current capability: ±50 mA into a 100 ohm load
- Low standby power dissipation: typically 60 mW at ±12V
- High input resistance: typically 2M at 25°C
- Full operating range: −55°C to +125°C
- Good high frequency response: unity gain at 30 MHz

With no external roll-off network, the amplifier is stable with a feedback ratio of 10 or greater. By adding a 200 pF capacitor between pins 9 and 10, and a 200 ohm resistor in series with a 75 pF capacitor from pin 4 to ground, the amplifier is stable to unity gain. The unity gain loop phase margin with the above compensation is typically 70 degrees. With a gain of 10 and no compensation the loop phase margin is typically 50 degrees.

Schematic and Connection Diagrams

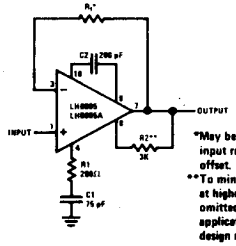




Order Number LH0005H or LH0005AH
See Package H10D

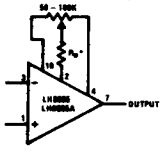
Typical Applications

Voltage Follower



*May be zero or equal to the input resistance for minimum offset.
**To minimize crossover distortion at higher frequencies. May be omitted for low frequency application or selected to suit design requirements

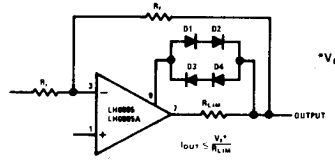
Offset Balancing Circuit



*Typical value, R_B = 100K. R_B may be increased for greater sensitivity with reduction in range.

*Previously called NH0005/NH0005A

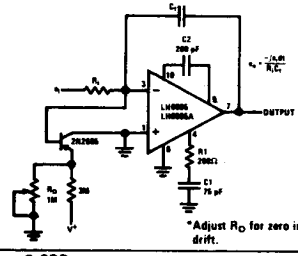
External Current Limiting



*V_f = Average forward voltage drop of diodes D_1 to D_4 at approx. 1 mA.

For continuous short circuit protection (V_S = ±12V, −55°C < T_A < +100°C) $R_{LIM} > 50\Omega$

Integrator with Bias Current Compensation



*Adjust R_D for zero integration drift.

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (see Curve)	400 mW
Differential Input Voltage	±15V
Input Voltage	Equal to supply voltages
Peak Load Current	±100 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

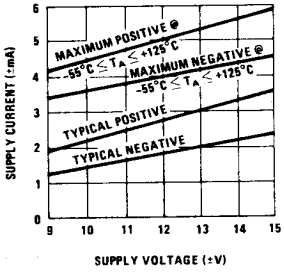
Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LH0005			LH0005A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage								
25°C	$R_S \leq 100\Omega$		5	10		1	3	mV
−55°C, 125°C	$R_S \leq 100\Omega$			10			4	mV
Input Offset Current								
25°C to 125°C			10	20		2	5	nA
−55°C			25	75		10	25	nA
Input Bias Current								
25°C to 125°C			15	50		8	25	nA
−55°C			100	250		60	125	nA
Large Signal Voltage Gain								
−55°C to 25°C	R_L = 10K, R2 = 3K, V_{OUT} = ±5V	2	4		4	5.5		V/mV
125°C		1.5	3		3	5		V/mV
Output Voltage Swing								
−55°C to 125°C	R_L = 10 kΩ	−10		+6	−10		+6	V
25°C to 125°C	R_L = 100Ω	−5		+5	−5		+5	V
−55°C	R_L = 100Ω	−4		+4	−4		+4	V
Input Resistance								
25°C		1	2		1	2		MΩ
Common Mode Rejection Ratio								
25°C	V_{IN} = ±4V, RS ≤ 100Ω	55	60		60	66		dB
Power Supply Rejection Ratio								
25°C		55	60		60	66		dB
Supply Current (+)								
−55°C to 125°C			3	5		3	5	mA
Supply Current (−)								
−55°C to 125°C			2	4		2	4	mA
Average Temperature Coefficient of Input Offset Voltage								
−55°C to 125°C	$R_S \leq 100\Omega$		20			10		uV/°C
Output Resistance								
25°C			70			70		Ω

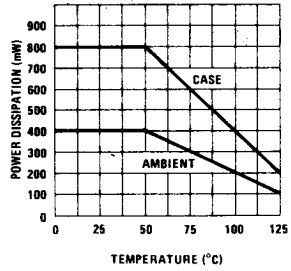
Note 1: These specifications apply for pin 6 grounded, V_S = ±12V, with Resistor R_1 = 200Ω in series with Capacitor C_1 = 75 pF from pin 4 to ground, and C_2 = 200 pF between pins 9 and 10 unless otherwise specified.

Guaranteed Performance Characteristics

Supply Current

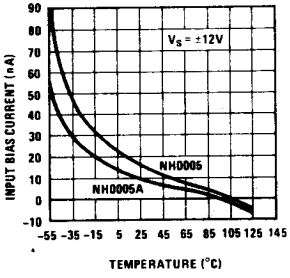


Maximum Power Dissipation

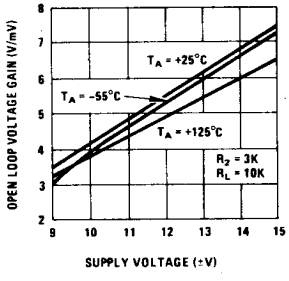


Typical Performance Characteristics

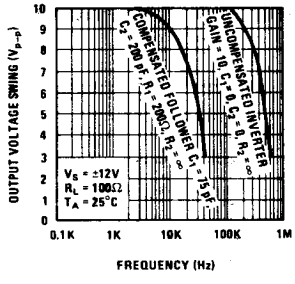
Input Bias Current



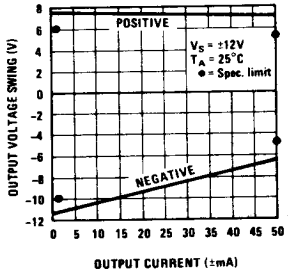
Voltage Gain



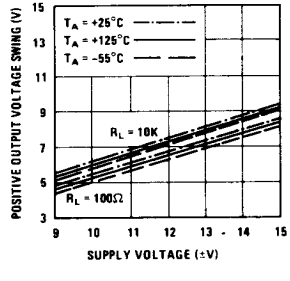
Loaded Output Voltage Swing



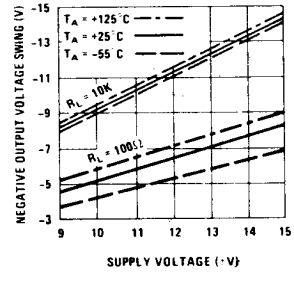
DC Output Voltage Swing



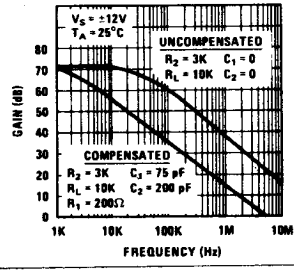
Positive Output Voltage Swing



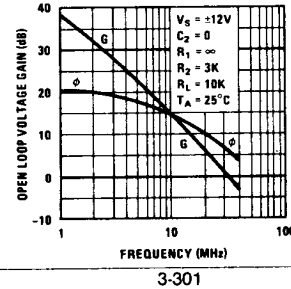
Negative Output Voltage Swing



Frequency Response



Open Loop Gain vs Excess Phase



Inverting Pulse Response