μA702
WIDEBAND DC AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA702 is a monolithic DC Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from dc to 30 MHz.

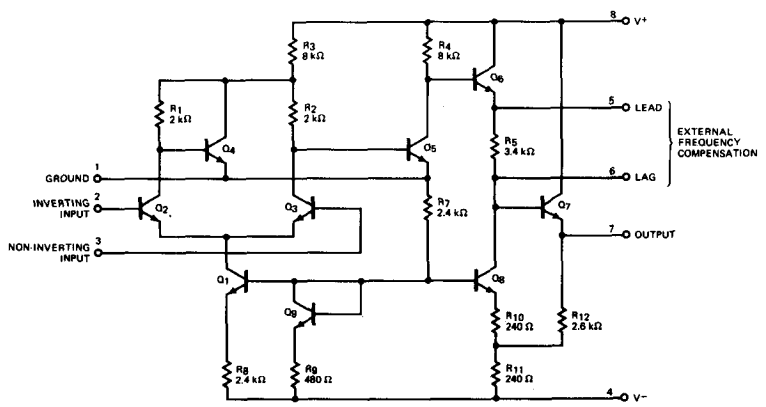
- **LOW OFFSET VOLTAGE**
- **LOW OFFSET VOLTAGE DRIFT**
- **WIDE BANDWIDTH – 20 MHz TYP**
- **HIGH SLEW RATE – 5 V/μs TYP**

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V– Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 V to –6.0 V
Internal Power Dissipation (Note)	
Metal Can	500 mW
DIP	670 mW
Flatpak	570 mW
Operating Temperature Range	
Military (μA702)	–55°C to +125°C
Commercial (μA702C)	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

NOTE
Rating applies to ambient temperature up to 70 C. Above 70°C ambient derate linearly at 6.3mW/°C for Metal Can, 8.3mW/°C for DIP and 7.1mW/°C for the Flatpak.

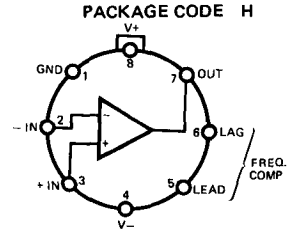
EQUIVALENT CIRCUIT



Pin numbers are shown for metal can only.

CONNECTION DIAGRAMS

8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

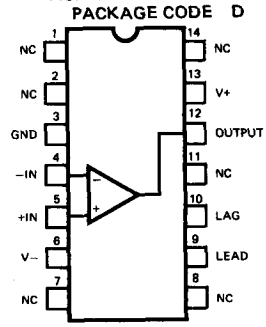


NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA702	μA702HM
μA702C	μA702HC

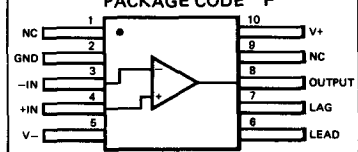
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA702	μA702DM
μA702C	μA702DC

10-LEAD FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
μA702	μA702FM

*Planar is a patented Fairchild process.

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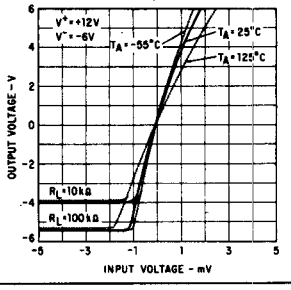
μA702

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

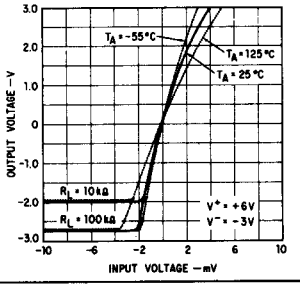
PARAMETER		CONDITIONS	V+ = 12.0V, V− = −6.0V			V+ = 6.0V, V− = −3.0V			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage		$R_S \leq 2\,k\Omega$		0.5	2.0		0.7	3.0	mV
Input Offset Current				180	500		120	500	nA
Input Bias Current				2.0	5.0		1.2	3.5	μA
Input Resistance			16	40		22	67		kΩ
Input Voltage Range			−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio		$R_S \leq 2\,k\Omega$, f ≤ 1 kHz	80	100		80	100		dB
Large Signal Voltage Gain		$R_L \geq 100\,k\Omega$, V_{OUT} = ±5.0 V	2500	3600	6000				
		$R_L \geq 100\,k\Omega$, V_{OUT} = ±2.5 V				600	900	1500	
Output Resistance				200	500		300	700	Ω
Supply Current		V_{OUT} = 0		5.0	6.7		2.1	3.3	mA
Power Consumption		V_{OUT} = 0		90	120		19	30	mW
Transient Response (unity-gain)	Rise Time	Cl = 0.01 μF, Rl = 20 Ω, $R_L \geq 100\,k\Omega$, V_{IN} = 10 mV		25	120				ns
	Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (x100 gain)	Rise Time	C3 = 50 pF, $R_L \geq 100\,k\Omega$,		10	30				ns
	Overshoot	V_{IN} = 1 mV		20	40				%
The following specifications apply for −55°C ≤ T_A ≤ +125°C:									
Input Offset Voltage		$R_S \leq 2\,k\Omega$			3.0			4.0	mV
Average Temperature Coefficient of Input Offset Voltage		R_S = 50 Ω, T_A = 25°C to +125°C		2.5	10		3.5	15	μV/°C
		R_S = 50 Ω, T_A = 25°C to −55°C		2.0	10		3.0	15	μV/°C
Input Offset Current		T_A = +125°C		80	500		50	500	nA
		T_A = −55°C		400	1500		280	1500	nA
Average Temperature Coefficient of Input Offset Current		T_A = 25°C to +125°C		1.0	5.0		0.7	4.0	nA/°C
		T_A = 25°C to −55°C		3.0	16		2.0	13	nA/°C
Input Bias Current		T_A = −55°C		4.3	10		2.6	7.5	μA
Input Resistance			6.0			8.0			kΩ
Common Mode Rejection Ratio		$R_S \leq 2\,k\Omega$, f ≤ 1 kHz	70	95		70	95		dB
Supply Voltage Rejection Ratio		V+ = 12 V, V− = −6.0 V to V+ = 6.0 V, V− = −3.0 V, $R_S \leq 2\,k\Omega$		75	200		75	200	μV/V
Large Signal Voltage Gain		$R_L \geq 100\,k\Omega$, V_{OUT} = ±5.0 V	2000		7000				
		$R_L \geq 100\,k\Omega$, V_{OUT} = ±2.5 V				500		1750	
Output Voltage Swing		$R_L \geq 100\,k\Omega$	±5.0	±5.3		±2.5	±2.7		V
		$R_L \geq 10\,k\Omega$	±3.5	±4.0		±1.5	±2.0		V
Supply Current		T_A = +125°C, V_{OUT} = 0		4.4	6.7		1.7	3.3	mA
		T_A = −55°C, V_{OUT} = 0		5.0	7.5		2.1	3.9	mA
Power Consumption		T_A = +125°C, V_{OUT} = 0		80	120		15	30	mW
		T_A = −55°C, V_{OUT} = 0		90	135		19	35	mW

TYPICAL PERFORMANCE CURVE FOR μA702

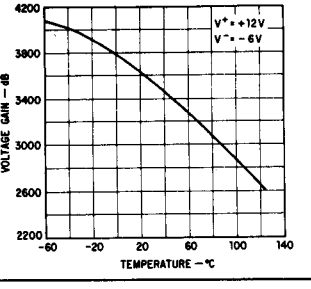
VOLTAGE TRANSFER CHARACTERISTIC



VOLTAGE TRANSFER CHARACTERISTIC

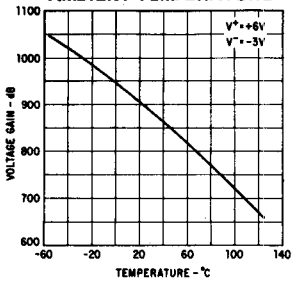


VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

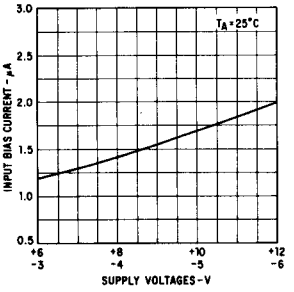


TYPICAL PERFORMANCE CURVES FOR μA702

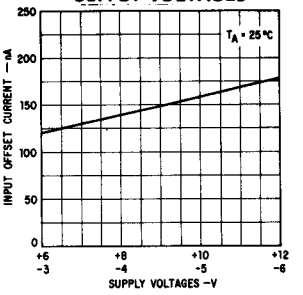
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



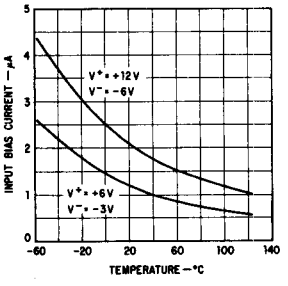
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



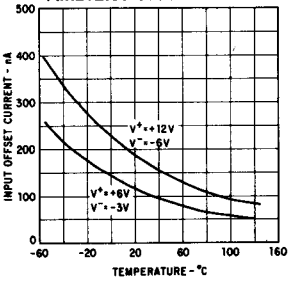
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



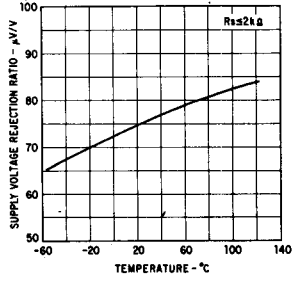
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



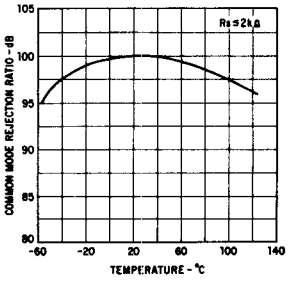
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



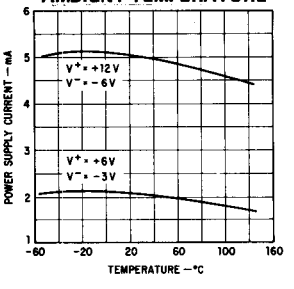
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



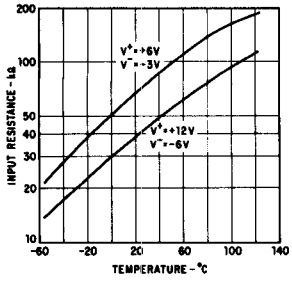
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



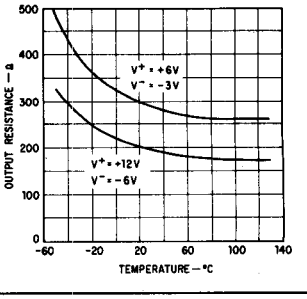
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

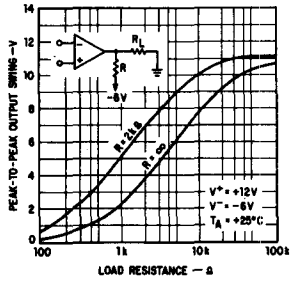


OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

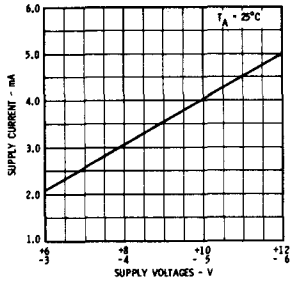


TYPICAL PERFORMANCE CURVES FOR μA702 AND μA702C

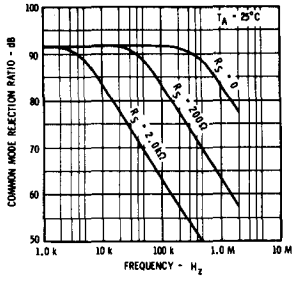
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



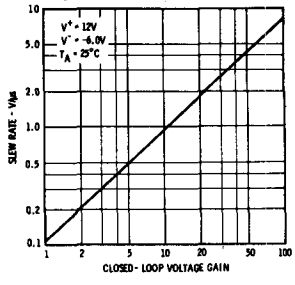
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



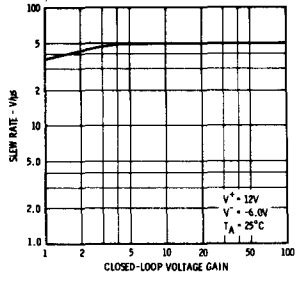
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



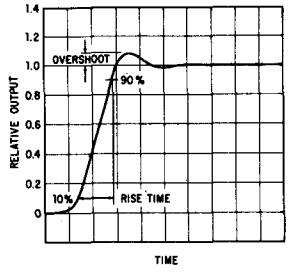
SLEW RATE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN (LAG COMPENSATION)



SLEW RATE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

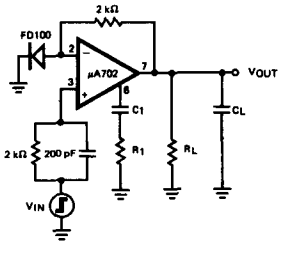


TRANSIENT RESPONSE

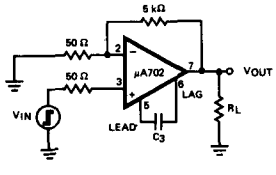


TRANSIENT RESPONSE TEST CIRCUITS

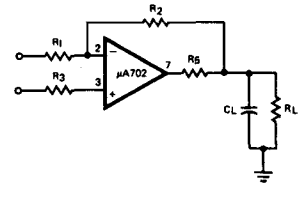
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



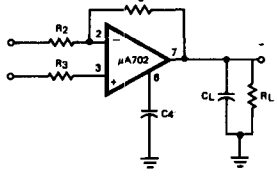
X100 AMPLIFIER (LEAD COMPENSATION)



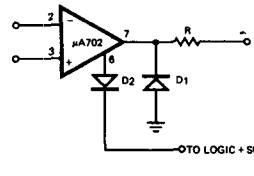
SERIES RESISTANCE LIMITING*



OUTPUT RISE TIME LIMITING*



LOGIC COMPATIBILITY



*Peak current limiting with capacitive loads.

Pin numbers are shown for metal can only.